AMENDMENTS TO THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-27. (Cancelled)

28. (Previously Presented) A system comprising:

a plurality of memory resources;

a plurality of peripheral resources;

a plurality of processors;

a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller for controlling access of said plurality of processors to said plurality of memory resources, wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second

communication, and wherein said first communication occurs simultaneously with said second communication; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller for controlling access of said plurality of processors to said plurality of peripheral resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

29. (Previously Presented) The system of Claim 28 further comprising:

a timer component coupled to said memory controller and said peripheral controller, said timer component for controlling timing of said memory controller and said peripheral controller.

30. (Cancelled)

31. (Previously Presented) The system of Claim 28, wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective peripheral resource of said plurality of peripheral resources.

32. (Previously Presented) The system of Claim 28, wherein said first and second resource controllers are further operable to enable said plurality of processors to perform apportioned operations in parallel.

33. (Previously Presented) The system of Claim 28 further comprising:

a semaphore component coupled to said plurality of processors and for enabling said plurality of processors to negotiate for access to at least one shared resource, wherein said at least one shared resource is selected from a group consisting of: a memory resource of said plurality of memory resources; and a peripheral resource of said plurality of peripheral resources.

34. (Previously Presented) The system of Claim 33, wherein said semaphore component is further operable to enable said plurality of processors to communicate with one another.

35. (Previously Presented) The system of Claim 33, wherein said access to said at least one shared resource is determined based upon information selected from a group consisting of: a chronological ordering of requests for a shared resource, a round-robin access arbitration scheme; a predetermined priority assignment of a given processor to at least one given shared resource; and a predetermined priority assignment of a given processor to at least one given shared resource for a predetermined period of time.

36. (Previously Presented) The system of Claim 28, wherein said plurality of memory resources, said plurality of peripheral resources, said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device.

37. (Previously Presented) A component for negotiating access to a plurality of shared resources, said component comprising:

a memory controller configured to couple at least one of a plurality of processors to at least one of a plurality of memory resources, wherein said memory controller comprises a first resource controller for controlling access of said plurality of processors to said plurality of memory resources, wherein said first resource controller is further operable to implement a first bus for enabling first communication between a first processor of said plurality of processors and a first memory resource of said plurality of memory resources, wherein said first resource controller is further operable to implement a second bus for enabling second communication between a second processor of said plurality of processors and a second memory resource of said plurality of memory resources, and wherein said first resource controller is further operable to implement said first and second buses for enabling said first communication to occur independently of said second communication; and

a peripheral controller coupled to said plurality of processors and a plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller for controlling access of said plurality of processors to said plurality of peripheral resources, wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources, and wherein said first communication occurs simultaneously with said second communication.

38. (Previously Presented) The component of Claim 37 further comprising:

a timer component coupled to said memory controller and said peripheral controller, said timer component for controlling timing of said memory controller and said peripheral controller.

39. (Cancelled)

40. (Previously Presented) The component of Claim 37, wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective peripheral resource of said plurality of peripheral resources.

41. (Previously Presented) The component of Claim 37, wherein said first and second resource controllers are further operable to enable said plurality of processors to perform apportioned operations in parallel.

42. (Previously Presented) The component of Claim 37 further comprising:

a semaphore component coupled to said plurality of processors and for enabling said plurality of processors to negotiate for access to at least one shared resource, wherein said at least one shared resource is selected from a group consisting of: said a memory resource of said plurality of memory resources; and a peripheral resource of said plurality of peripheral resources.

43. (Previously Presented) The component of Claim 42, wherein said semaphore component is further operable to enable said plurality of processors to communicate with one another.

44. (Previously Presented) The component of Claim 42, wherein said access to said at least one shared resource is determined based upon information selected from a group consisting of: a chronological ordering of requests for a shared resource; a round-robin access arbitration scheme; a predetermined priority assignment of a given processor to at least one given shared resource; and a predetermined priority assignment of a given processor to at least one given shared resource for a predetermined period of time.

45. (Previously Presented) The component of Claim 37, wherein said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device.

46. (Previously Presented) A controller for negotiating access to a plurality of shared resources, said controller comprising:

a plurality of shared resource controllers, wherein each of said plurality of shared resource controllers is operable to simultaneously communicate with a respective shared resource of a plurality of shared resources;

a plurality of dedicated buses, wherein each of said plurality of dedicated buses is coupled to a respective shared resource controller of said plurality of shared resource controllers, and wherein each of said plurality of dedicated

buses is further operable to couple to a respective shared resource of said plurality of shared resources; and

a resource arbitration controller for controlling access of a plurality of processors to said plurality of shared resources, wherein said resource arbitration controller is further operable to control a first switching component for enabling a first communication between a first processor of said plurality of processors and a first shared resource controller of said plurality of shared resource controllers, wherein said resource arbitration controller is further operable to control a second switching component for enabling a second communication between a second processor of said plurality of processors and a second shared resource controller of said plurality of shared resource controllers, wherein said resource arbitration controller is further operable to control said first and second switching components for enabling said first communication to occur independently of said second communication, and wherein said resource arbitration controller is further operable to control said first and second switching components based upon a respective priority value assigned to each of said first and second processors.

47. (Previously Presented) The controller of Claim 46, wherein said priority value is assigned to said processor by a semaphore component coupled to said resource arbitration controller and said plurality of processors.

48. (Previously Presented) The controller of Claim 46, wherein said plurality of shared resources are selected from a group consisting of: memory resources; and peripheral resources.

49. (Previously Presented) The controller of Claim 46, wherein said resource arbitration controller is further operable to control said first and second switching components for enabling said first communication to occur simultaneously with said second communication.

50. (Previously Presented) The controller of Claim 46, wherein said resource arbitration controller is further operable to enable said plurality of processors to perform apportioned operations in parallel.

51. (Previously Presented) The controller of Claim 46, wherein said plurality of shared resource controllers, said plurality of dedicated buses, and said resource arbitration controller comprise components of a portable electronic device.

52. (New) The system of Claim 28, wherein said memory controller is further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks.